DTM67220

1GB 200-Pin 1Rx8 Unbuffered Non-ECC DDR2 SO-DIMM

Identification

DTM67220 128Mx64

1GB 1Rx8 PC2-6400S-666-12-F1

Performance range

Clock/ Module Speed/ CL-t_{RCD} -t_{RP}

400 MHz / PC2-6400 / 6-6-6

333 MHz / PC2-5300 / 5-5-5

266 MHz / PC2-4200 / 4-4-4

Features

- 200-pin JEDEC SO-DIMM Dual-sided assembly 67.600mm [2.661”] wide by 30.0mm [1.181”] high
- Operating Voltage: 1.8 V ±0.1
- I/O Type: SSTL_18
- Data Transfer Rate: 6.4 Gigabytes/sec
- Bursts Length: 4 and 8.
- CAS Latencies: 4, 5 and 6
- Programmable I/O driver strength (OCD)
- Programmable On-Die Termination (ODT)
- Differential/Redundant Data Strobe signals
- SDRAM Addressing (Row/Col/Bank): 14/10/3
- One Physical Rank
- Fully RoHS Compliant

Description

The DTM67220 assembly is a 128Mx64bit Unbuffered Non-ECC memory module, which conforms to JEDEC's DDR2, PC2-6400 standard. The assembly consists of one rank comprised of eight 128Mx8 DDR2 SDRAMs in a 60 Ball FBGA package.

A 2Kbit EEPROM for serial presence detect provides critical timing and configuration information used by the system to identify and configure the memory.

The assembly is a Small Outline Dual In-line Memory Module intended for mounting into 200-pin edge connector sockets.

Pin Configurations

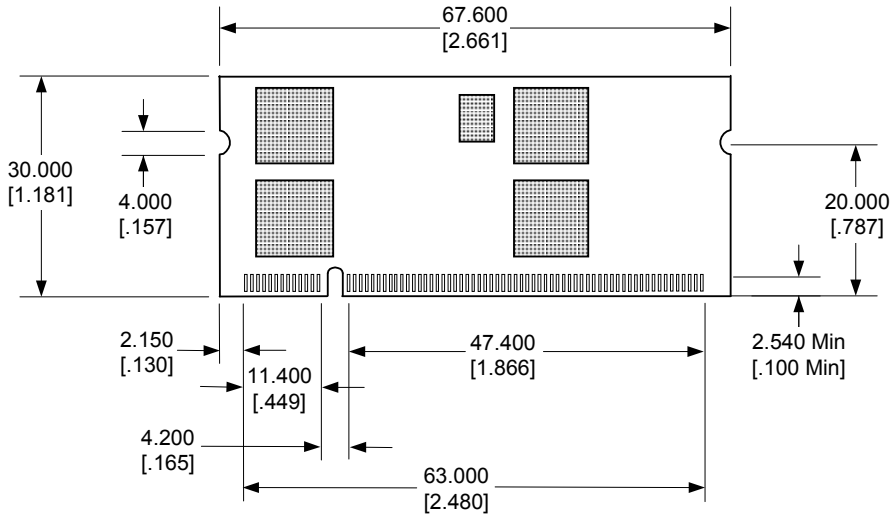
Front side												Back side											
1	V_{REF}	51	DQS2	101	A1	151	DQ42	2	V_{SS}	52	DM2	102	A0	152	DQ46
3	V_{SS}	53	V_{SS}	103	V_{DD}	153	DQ43	4	DQ4	54	V_{SS}	104	V_{DD}	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	V_{SS}	6	DQ5	56	DQ22	106	BA1	156	V_{SS}
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	V_{SS}	58	DQ23	108	/RAS	158	DQ52
9	V_{SS}	59	V_{SS}	109	/WE	159	DQ49	10	DM0	60	V_{SS}	110	/S0	160	DQ53
11	/DQS0	61	DQ24	111	V_{DD}	161	V_{SS}	12	V_{SS}	62	DQ28	112	V_{DD}	162	V_{SS}
13	DQS0	63	DQ25	113	/CAS	163	NC	14	DQ6	64	DQ29	114	ODT	164	CK1
15	V_{SS}	65	V_{SS}	115	/S1*	165	V_{SS}	16	DQ7	66	V_{SS}	116	A13	166	/CK1
17	DQ2	67	DM3	117	V_{DD}	167	/DQS6	18	V_{SS}	68	DQS3	118	V_{DD}	168	V_{SS}
19	DQ3	69	NC	119	ODT1*	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	V_{SS}	71	V_{SS}	121	V_{SS}	171	V_{SS}	22	DQ13	72	V_{SS}	122	V_{SS}	172	V_{SS}
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	V_{SS}	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	V_{SS}	77	VSS	127	V_{SS}	177	V_{SS}	28	V_{SS}	78	V_{SS}	128	V_{SS}	178	V_{SS}
29	/DQS1	79	CKE0	129	/DQS4	179	DQ56	30	CK0	80	CKE1*	130	DM4	180	DQ60
31	DQS1	81	V_{DD}	131	DQS4	181	DQ57	32	/CK0	82	V_{DD}	132	V_{SS}	182	DQ61
33	V_{SS}	83	NC	133	V_{SS}	183	V_{SS}	34	V_{SS}	84	NC/A15*	134	DQ38	184	V_{SS}
35	DQ10	85	NC	135	DQ34	185	DM7	36	DQ14	86	NC/A14*	136	DQ39	186	/DQS7
37	DQ11	87	V_{DD}	137	DQ35	187	V_{SS}	38	DQ15	88	V_{DD}	138	V_{SS}	188	DQS7
39	V_{SS}	89	A12	139	V_{SS}	189	DQ58	40	V_{SS}	90	A11	140	DQ44	190	V_{SS}
41	V_{SS}	91	A9	141	DQ40	191	DQ59	42	V_{SS}	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	V_{SS}	44	DQ20	94	A6	144	V_{SS}	194	DQ63
45	DQ17	95	V_{DD}	145	V_{SS}	195	SDA	46	DQ21	96	V_{DD}	146	/DQS5	196	V_{SS}
47	V_{SS}	97	A5	147	DM5	197	SCL	48	V_{SS}	98	A4	148	DQS5	198	SA0
49	/DQS2	99	A3	149	V_{SS}	199	V_{DD}SPD	50	/Event*	100	A2	150	V_{SS}	200	SA1

* = not used on the DTM67220

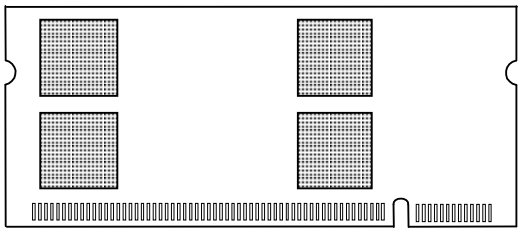
Pin Names

Pin name	Function
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write enable
/S[1:0]	Chip select input
CK[1:0], /CK[1:0]	Differential Clock inputs
CKE[1:0]	Clock enable input
BA[2:0]	Bank select input
A[15:0]	Address input (Multiplexed)
ODT[1:0]	On Die Termination
DQS[7:0], /DQS[7:0]	Data strobes
DM[7:0]	Data masks
DQ[63:0]	Data I/Os: Data bus
SCL	Serial clock
SDA	Serial data I/O
SA[1:0]	Address EEPROM
/Event	Temperature sensing
VREF	Reference voltage.
VDD	Power supply: 1.8V +/- 0.1V
VSS	Ground
VDDSPD	Serial EEPROM power supply
NC	No connects

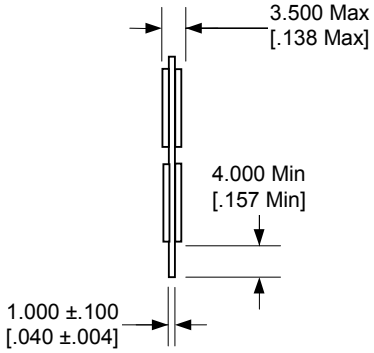
Front view



Back view



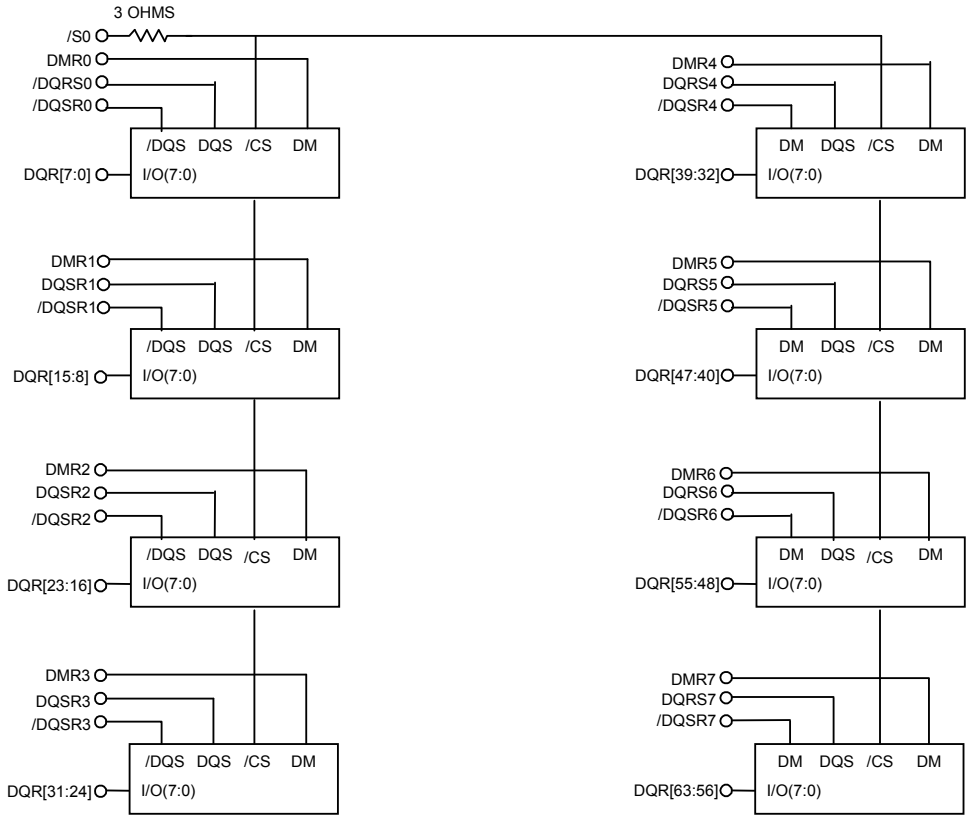
Side view

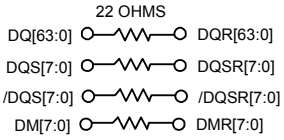


Notes

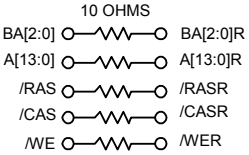
Tolerances on all dimensions except where otherwise indicated are ± .13 [.005].

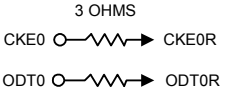
All dimensions are expressed: millimeters [inches].

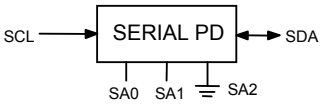


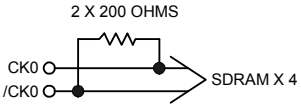


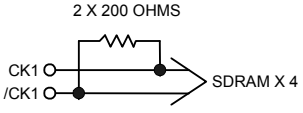
GLOBAL SDRAM CONNECTS

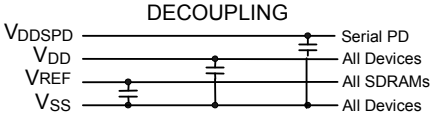












Absolute Maximum Ratings
(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Ambient Temperature, Operating	T_A	0	70	C
DRAM Case Temperature, Operating	T_{CASE}	0	85*	C
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.5	2.3	V
Voltage on Any Pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5	2.3	V

*95C at 2x Refresh

Recommended DC Operating Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
I/O Reference Voltage	V_{REF}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1
Bus Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	

Notes:
1. The value of V_{REF} is expected to equal one-half V_{DD} and to track variations in the V_{DD} DC level. Peak-to-peak noise on V_{REF} may not exceed ±1% of its DC value.

DC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	V_{REF} + 0.125	V_{DD} + 0.300	V
Logical Low (Logic 0)	$V_{IL(DC)}$	-0.300	V_{REF} - 0.125	V

AC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	V_{REF} + 0.250	-	V
Logical Low (Logic 0)	$V_{IL(AC)}$	-	V_{REF} - 0.250	V

Differential Input Logic Levels (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
DC Input Signal Voltage	$V_{IN(DC)}$	-0.300	V_{DD} + 0.300	V	1
DC Differential Input Voltage	$V_{ID(DC)}$	-0.250	V_{DD} + 0.600	V	2
AC Differential Input Voltage	$V_{ID(AC)}$	-0.500	V_{DD} + 0.600	V	3
AC Differential Cross-Point Voltage	$V_{IX(AC)}$	0.50 VDD - 0.175	0.50 VDD + 0.175	V	4

Notes:
1. $V_{IN(DC)}$ specifies the allowable DC excursion of each input of a differential pair.
2. $V_{ID(DC)}$ specifies the input differential voltage, *i.e.* the absolute value of the difference between the two voltages of a differential pair.
3. $V_{ID(AC)}$ specifies the input differential voltage required for switching.
4. The typical value of $V_{IX(AC)}$ is expected to be 0.5 V_{DD} and is expected to track variations in V_{DD}.

Capacitance (T_A = 25 C, f = 100 MHz)

PARAMETER	Pin	Symbol	Min.	Max.	Unit
Input Capacitance, Clock	CK[1:0], /CK[1:0]	CIN1	4	8	pF
Input Capacitance, Address and Control	BA[2:0], A[13:0], /RAS, /CAS, /WE, ODT0, CKE0, /S0	CIN2	8	14	pF
Input/Output Capacitance	DQ[63:0], DQS[7:0], /DQS[7:0], DM[7:0]	CIO	2.5	3.5	pF

DC Characteristics (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current Command and Address	I_{LI}	-80	80	µA	1
Input Leakage Current /S0, CKE0, ODT0	I_{LI}	-40	40	µA	1
Input Leakage Current CK[1:0], /CK[1:0]	I_{LI}	-30	30	µA	1
Input Leakage Current DM	I_{LI}	-10	10	µA	1
Output Leakage Current DQS, DQ	I_{OZ}	-10	10	µA	2
Output Minimum Source DC Current	I_{OH}	-13.4	-	mA	3
Output Minimum Sink DC Current	I_{OL}	+13.4	-	mA	4

Notes:
1. These values are guaranteed by design and are tested on a sample basis only
2. DQx and ODT are disabled, and 0 V ≤ V_{OUT} ≤ V_{DD}.
3. V_{DD} = 1.7 V, V_{OUT} = 1420 mV. (V_{OUT} - V_{DD})/I_{OH} must be less than 21 Ohms for values of V_{OUT} between V_{DD} and (V_{DD} - 280 mV).
4. V_{DD} = 1.7 V, V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 Ohms for values of V_{OUT} between 0 V and 280 mV.

I_{DD} Specifications and Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	$I_{DD}0$	CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching.	360	mA
Operating One Bank Active-Read-Precharge Current	$I_{DD}1$	I_{OUT} = 0 mA; BL = 4, CL = 5 ns, AL = 0; CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching.	408	mA
Precharge Power-Down Current	$I_{DD}2P$	All banks idle; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating.	80	mA
Precharge Quiet Standby Current	$I_{DD}2Q$	All banks idle; CKE is HIGH, /CS is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating.	160	mA
Precharge Standby Current	$I_{DD}2N$	All banks idle; CKE is HIGH, /CS is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching.	200	mA
Active Power-Down Current	$I_{DD}3P$	All banks open; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating. Fast Power-down exit (Mode Register bit 12 = 0)	184	mA
Active Standby Current	$I_{DD}3N$	All banks open; t_{RAS} = 70 ms; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching.	296	mA
Operating Burst Write Current	$I_{DD}4W$	All banks open, Continuous burst writes; BL = 4, CL = 5 t_{CK}, AL = 0; t_{RAS} = 70 ms, CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching.	576	mA
Operating Burst Read Current	$I_{DD}4R$	All banks open, Continuous burst reads, I_{OUT} = 0 mA; BL = 4, CL = 5 t_{CK}, AL = 0, t_{RAS} = 70 ms; CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching.	640	mA
Burst Refresh Current	$I_{DD}5$	Refresh command at every 75 ns; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching.	840	mA
Self Refresh Current	$I_{DD}6$	CK and /CK at 0 V; CKE ≤ 0.2 V; Other control and address bus inputs are floating; Data bus inputs are floating.	80	mA
Operating Bank Interleave Read Current	$I_{DD}7$	All bank interleaving reads, I_{OUT}= 0 mA; BL = 4, CL = 5 t_{CK}; AL = 70 ns; t_{RRD} = 7.5 ns; CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching.	1280	mA

Note: For all $I_{DD}X$ measurements, t_{CK} = 2.5 ns, t_{RC} = 60 ns, t_{RCD} = 15 ns, t_{RAS} = 45 ns, and t_{RP} = 15 ns unless otherwise specified. All currents are based on DRAM absolute maximum values.

AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
DQ Output Access Time from Clock	t_{AC}	-400	+400	ps
CAS-to-CAS Command Delay	t_{CCD}	2	-	t_{CK}
Clock High Level Width	t_{CH}	0.48	0.52	t_{CK}
Clock Cycle Time	t_{CK}	2500	8000	ps
Clock Low Level Width	t_{CL}	0.48	0.52	t_{CK}
Data Input Hold Time after DQS Strobe	t_{DH}	125	-	ps
DQ Input Pulse Width	t_{DIPW}	0.35	-	t_{CK}
DQS Output Access Time from Clock	t_{DQSCK}	-350	+350	ps
Write DQS High Level Width	t_{DQSH}	0.35	-	t_{CK}
Write DQS Low Level Width	t_{DQSL}	0.35	-	t_{CK}
DQS-Out Edge to Data-Out Edge Skew	t_{DQSQ}	-	200	ps
Data Input Setup Time Before DQS Strobe	t_{DS}	50	-	ps
DQS Falling Edge from Clock, Hold Time	t_{DSH}	0.2	-	t_{CK}
DQS Falling Edge to Clock, Setup Time	t_{DSS}	0.2	-	t_{CK}
Clock Half Period	t_{HP}	minimum of t_{CH} or t_{CL}	-	ns
Address and Command Hold Time after Clock	t_{IH}	250	-	ps
Address and Command Setup Time before Clock	t_{IS}	175	-	ps
Load Mode Command Cycle Time	t_{MRD}	2	-	t_{CK}
DQ-to-DQS Hold	t_{QH}	t_{HP} - t_{QHS}	-	-
Data Hold Skew Factor	t_{QHS}	-	400	ps
Active-to-Precharge Time	t_{RAS}	45	70K	ns
Active-to-Active / Auto Refresh Time	t_{RC}	60	-	ns
RAS-to-CAS Delay	t_{RCD}	15	-	ns
Average Periodic Refresh Interval	t_{REFI}	-	7.8	µs
Auto Refresh Row Cycle Time	t_{RFC}	127.5	-	ns
Row Precharge Time	t_{RP}	15	-	ns
Read DQS Preamble Time	t_{RPRE}	0.9	1.1	t_{CK}
Read DQS Postamble Time	t_{RPST}	0.4	0.6	t_{CK}
Row Active to Row Active Delay	t_{RRD}	7.5	-	ns
Internal Read to Precharge Command Delay	t_{RTP}	7.5	-	ns
Write DQS Preamble Time	t_{WPRE}	0.35	-	t_{CK}
Write DQS Postamble Time	t_{WPST}	0.4	0.6	t_{CK}
Write Recovery Time	t_{WR}	15	-	ns
Internal Write to Read Command Delay	t_{WTR}	7.5	-	ns
Exit Self Refresh to Non-Read Command	t_{XSNR}	t_{RFC}(min) + 10	-	ns
Exit Self Refresh to Read Command	t_{XSRD}	200	-	t_{CK}

SERIAL PRESENCE DETECT MATRIX

Byte#	Function.	Value	Hex
0	Number of Bytes Utilized by Module Manufacturer	128 bytes	0x80
1	Total number of Bytes in Serial PD device	256 bytes	0x08
2	Memory Type	DDR2 SDRAM	0x08
3	Number of Row Addresses	14	0x0E
4	Number of Column Addresses	10	0x0A
5	Module Attributes - Number of Ranks, Package and Height		0x60
	# of Ranks -	1	
	Card on Card -	No	
	DRAM Package -	Planar	
	Module Height -	30mm	
6	Module Data Width.	64	0x40
7	Reserved	UNUSED	0x00
8	Voltage Interface Level of this assembly	SSTL/1.8V	0x05
9	SDRAM Cycle time. (Max. Supported CAS Latency). CL=X (tCK) ns	2.5	0x25
10	SDRAM Access from Clock. (Highest CAS latency). (tAC) ns	0.4	0x40
11	DIMM configuration type (Non-parity, Parity or ECC)		0x00
	Data Parity -		
	Data ECC -		
	Address/Command Parity -		
	TBD -		
	TBD -		
	TBD -		
	TBD -		
	TBD -		
12	Refresh Rate/Type (us)	7.8 (SR)	0x82
13	Primary SDRAM Width	8	0x08
14	Error Checking SDRAM Width	None	0x00
15	Reserved	UNUSED	0x00
16	SDRAM Device Attributes: Burst Lengths Supported		0x0C
	TBD -		
	TBD -		
	Burst Length = 4 -	X	
	Burst Length = 8 -	X	
	TBD -		
	TBD -		
	TBD -		
	TBD -		
17	SDRAM Device Attributes - Number of Banks on SDRAM Device	8	0x08
18	SDRAM Device Attributes: CAS Latency		0x70

	TBD -		
	TBD -		
	Latency = 2 -		
	Latency = 3 -		
	Latency = 4 -	X	
	Latency = 5 -	X	
	Latency = 6 -	X	
	TBD -		
19	DIMM Mechanical Characteristics. Max. module thickness. (mm)	x </= 3.80	0x01
20	DIMM type information		0x04
	Regular RDIMM (133.35mm) -		
	Regular UDIMM (133.35mm) -		
	SODIMM (67.6mm) -	X	
	Micro-DIMM (45.5mm) -		
	Mini RDIMM (82.0mm) -		
	Mini UDIMM (82.0mm) -		
	TBD -		
	TBD -		
21	SDRAM Module Attributes (Refer to Byte20 for DIMM type information).		0x00
	Number of active registers on the DIMM (N/A for UDIMM) -	1	
	Number of PLL on the DIMM (N/A for UDIMM) -	0	
	FET Switch External Enable -	No	
	TBD -		
	Analysis probe installed -	No	
	TBD -		
22	SDRAM Device Attributes: General		0x03
	Includes Weak Driver -	X	
	Supports 50 ohm ODT -	X	
	Supports PASR (Partial Array Self Refresh) -		
	TBD -		
	TBD -		
	TBD -		
	TBD -		
	TBD -		
23	Minimum Clock Cycle Time at Reduced CAS Latency, CL = X-1 (ns)	3	0x30
24	Maximum Data Access Time (tAC) from Clock at CL = X- 1 (ns)	0.4	0x40
25	Minimum Clock Cycle Time at CL = X-2 (ns)	3.75	0x3D
26	Maximum Data Access Time (tAC) from Clock at CL = X-2 (ns)	0.4	0x40
27	Minimum Row Precharge Time (tRP) (ns)	15	0x3C
28	Minimum Row Active to Row Active Delay (tRRD) (ns)	7.5	0x1E
29	Minimum RAS to CAS Delay (tRCD) (ns)	15	0x3C
30	Minimum Active to Precharge Time (tRAS) (ns)	45	0x2D
31	Module Rank Density	1GB	0x01

32	Address and Command Setup Time Before Clock (tIS) (ns)	0.17	0x17
33	Address and Command Hold Time After Clock (tIH) (ns)	0.25	0x25
34	Data Input Setup Time Before Strobe (tDS) (ns)	0.05	0x05
35	Data Input Hold Time After Strobe (tDH) (ns)	0.12	0x12
36	Write Recovery Time (tWR) (ns)	15	0x3C
37	Internal write to read command delay (tWTR) (ns)	7.5	0x1E
38	Internal read to precharge command delay (tRTP) (ns)	7.5	0x1E
39	Memory Analysis Probe Characteristics.	UNUSED	0x00
40	Extension of Byte 41(tRC) and Byte 42 (tRFC) (ns)		0x06
	Add this value to byte 41 -	0	
	Add this value to byte 42 -	0.5	
41	SDRAM Device Minimum Active to Active/Auto Refresh Time (tRC) (ns)	60	0x3C
42	SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC). (ns)	127.5	0x7F
43	SDRAM Device Maximum Cycle Time (tCK max). (ns)	8	0x80
44	SDRAM Dev DQS-DQ Skew for DQS & DQ signals (tDQSQ) (ns)	0.2	0x14
45	DDR SDRAM Device Read Data Hold Skew Factor (tQHS) (ns)	0.3	0x1E
46	PLL Relock Time (us)	UNUSED	0x00
47	DRAM maximum Case Temperature Delta. (Degree C).		0x00
	DT4R4W Delta (Bits 0:3) -	0	
	Tcasemax delta (Bits 7:4) -	0	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM). (C/Watt)	58	0x74
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/ Mode Bits (DT0/Mode Bits). (Degree C).		0x58
	Bit 0. If "0" DRAM does not support high temperature self-refresh entry -	0	
	Bit 1. If "0" Do not need double refresh rate for the proper operation -	0	
	DT0, (Bits 2:7) -	6.6	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q). (Degree C).	4.4	0x2C
51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down (DT2P). (Degree C).	0.765	0x33
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N). (Degree C).	6	0x28
53	DRAM Case temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast). (Degree C).	3.3	0x42

54	DRAM Case temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow). (Degree C).	1.1	0x2C
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit). (Degree C).		0x4A
	Bit 0. "0" if DT4W is greater than DT4R -	0	
	DT4R, (Bits 1:7) -	14.8	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B). (Degree C).	23.5	0x2F
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7). (Degree C).	31	0x3E
58	Thermal Resistance of PLL Package from Top to Ambient (Psi T-A PLL). (C/Watt).	UNUSED	0x00
59	Thermal Resistance of Register Package from Top to Ambient (Psi T-A Register). (C/Watt).	UNUSED	0x00
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active). (Degree C).	UNUSED	0x00
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit).		0x00
	Bit 0.If "0"Unit for Bits 2:7 is 0.75C -	0.75	
	Bit 1. RFU. Default: 0 -	0	
	Register Active,(Bits 2:7) -	0	
62	SPD Revision	Revision 1.2	0x12
63	Checksum for Bytes 0-62		0x41
64	Module Manufacturer's JEDEC ID Code	Dataram ID	0x7F
65	Module Manufacturer's JEDEC ID Code	Dataram ID	0x91
66-71	Module Manufacturer's JEDEC ID Code	UNUSED	0x00
72	Module Manufacturing Location	UNUSED	0x00
73	Module Part Number	D	0x44
74	Module Part Number	A	0x41
75	Module Part Number	T	0x54
76	Module Part Number	A	0x41
77	Module Part Number	R	0x52
78	Module Part Number	A	0x41
79	Module Part Number	M	0x4D
80	Module Part Number		0x20
81	Module Part Number	6	0x36
82	Module Part Number	7	0x37

83	Module Part Number	2	0x32
84	Module Part Number	2	0x32
85	Module Part Number	0	0x30
86-90	Module Part Number		0x20
91,92	Module Revision Code	UNUSED	0x00
93,94	Module Manufacturing Date	UNUSED	0x00
95	Module Serial Number	S	0x53
96	Module Serial Number	E	0x45
97	Module Serial Number	R	0x52
98	Module Serial Number	#	0x23
99-127	Manufacturer's Specific Data	UNUSED	0x00

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